REMARKS

The non-final Office Action mailed on June 21, 2004, has been received and its contents carefully considered.

Claims 1 and 3-20 are currently pending in this application, with claims 1, 3, 4 and 8 being the independent claims.

The Applicants note with appreciation the Examiner's indication in the Action that claims 5-7 would be allowable if rewritten in independent form including all of the limitations of their respective base claims and any intervening claims.

In this Amendment, claims 1, 3-8, 16 and 18-20 are amended to more clearly recite the claimed invention. In addition, claim 4 is amended to more clearly distinguish over the applied references.

In the Action, claims 1, 4, 9, 11, 17-18 and 20 are rejected under 35 USC §103(a) as being obvious over *Tzu* (U.S. Patent No. 6,201,302) in view of *Rolda, Jr. et al.* (U.S. Pat. Publ. No. 2002/0030261). Claims 3, 8, 10, 12-16 and 19 stand rejected under 35 USC §103(a) as being obvious over *Tzu* in view of *Rolda, Jr. et al.*, and further in view of *Tao et al.* (U.S. Patent No. 6,118,176). Except to the extent addressed by the claim amendments made herein, the rejections are respectfully traversed.

A feature of the semiconductor chip package of the present invention recited in the independent claims is that the package comprises an interposer made of an insulating material on one surface of which a lead portion is provided, and on another surface of which external terminals are provided. Further, a through-hole is formed in the interposer.

In the invention recited in claims 1 and 8, second electrodes formed on a second integrated semiconductor chip, and external terminals on the interposer, are electrically connected to each other via the through-hole.

In the invention recited in claim 3, the second integrated semiconductor chip (lower chip of the package) is provided in the through-hole using an adhesive sheet. The second electrodes on the second integrated semiconductor chip and the external terminals on the interposer are electrically connected to each other.

In the invention recited in claim 4, as amended, two chips with different sizes are prepared. The lower, second chip is provided in the through-hole. An adhesive sheet is used

to mount the first chip to the substrate and the two chips to each other. The second electrodes on the second chip and the external terminals formed on the lower surface of the interposer are electrically connected to each other.

In other words, the present invention has one basic configuration in which the first and second chips are provided on the upper surface of the interposer (claims 1 and 8), and another configuration in which a first chip is provided on the upper surface of the interposer, and the second chip is provided in the through-hole via the adhesive sheet provided on the lower surface of the first chip (claims 3 and 4). In both of these configurations, the second electrodes on the second chip and the external terminals on the interposer are electrically connected to each other. Advantageously, this allows wiring for electrical connections of the second electrodes and the external terminals to be formed in a stable manner, which results in a semiconductor device package having high reliability.

Specifically, the number of external terminals increases when two chips are provided in one package. This requires narrower leads and narrower pitches between the leads, which may cause misconnections and short circuits occurring between the leads. However, these problems can be avoided by the configurations of the present inventions described above, since electrical connections of external terminals with the first electrodes on the first chip and the second electrodes on the second chip are arranged on opposite sides of the interposer. Accordingly, a semiconductor device package having high reliability can be obtained.

In the Action, the Examiner points to *Tzu* as disclosing a semiconductor package having multiple chips where, in Figure 3, semiconductor chips 306 and 312 are mounted on a substrate 302 in a reverse manner with wiring 310 connecting the lower semiconductor chip 312 to the substrate 302. However, *Tzu* fails to disclose the configuration recited in claims 1 and 8 of the present invention in which the second chip is mounted on the first surface of the interposer substrate with the one side of the second chip facing the first surface of the interposer substrate, such that the second electrode on the one side of the second chip is exposed through the through-hole in the interposer substrate for wiring to external terminals on the second surface of the interposer substrate. Rather, as the Examiner indicates in the Action, Figure 3 of *Tzu* discloses that the semiconductor substrate 302 has an opening larger than the lower chip 312 but smaller than the upper chip 306.

In the Action, the Examiner acknowledges that *Tzu* fails to disclose the required insulating interposer between the two chips. To cure this deficiency in *Tzu*, the Examiner points to the *Rolda* reference as disclosing a multi-flip-chip semiconductor assembly where in Figure 1, the element 12 that is between the semiconductor chips 110 and 130 is an insulating interposer.

Rolda, in Figure 1, discloses a semiconductor assembly in which two chips 110 and 130, each having an active surface including integrated circuits and a plurality of input/output solder ball contacts, are mounted face-to-face, rather than back-to-back, on opposite surfaces of the interposer substrate 120. *Rolda* totally fails to teach or suggest forming a through-hole in the substrate 120, as the independent claims require. Thus it appears that the Examiner has engaged in piecemeal reconstruction of the claimed invention, picking and choosing from the *Rolda* reference only so much of it as will support a given a position, to the exclusion of other parts necessary to the full appreciation of what *Rolda* would fairly suggest to one of ordinary skill in the art. It is respectfully submitted that even if the inventions of the *Tzu* and *Rolda* references were combined as suggested by the Examiner, a structure having the features recited in the claims would not be achieved.

In the invention recited in claims 3 and 4, an adhesive sheet covers the through-hole in the interposer substrate. In the Action, the Examiner acknowledges that *Tzu* fails to disclose the required adhesive sheet. Examiner points to *Tao*, in figure 4, as disclosing the elements 404 and 405 that are adhesive layers.

The cited *Tao* reference discloses a multi-chip technique in a LOC (lead on chip) structure. *Tao* does not teach or even suggest providing an interposer substrate. The adhesive layers to which the Examiner refers are used in *Tao* to mount the chips to each other and to the lead frame. Accordingly, is respectfully submitted that even a person skilled in the art would not be motivated to achieve the present invention by combining the inventions disclosed in the applied references.

The Applicants note that *Tzu* discloses a configuration in which a <u>conductive</u> plate 402 is used to mount the first die 306 and the second die 312 on the opposite side of the plate 402 (Fig. 4). The conductive plate 402 has the potential for causing short circuits between neighboring wires 310 via the plate 402. In contrast, in the present invention recited in claim 3, such a problem will not occur, since an <u>insulating</u> sheet is used.

In addition, in the configurations shown in Figs. 3 and 4 of *Tzu*, a heat sink 318 is used. Therefore, short circuits between neighboring wires 310 may occur via the heat sink 318. Further, stable connections by wires may be inhibited, since a portion overlapped by the heat sink 318, which includes the wires leads 310 and connection portions, is not molded by the resin 316.

In contrast, in the present invention, all of the chips, the electrodes, and the connection portions are covered by resin. Therefore, the above problems will not occur.

For at least the foregoing reasons, is respectfully submitted that claims 1, 3, 4 and 8, as well as claims 9-20, patentably distinguish over the applied art references, whether considered individually or in combination. The obviousness rejections accordingly should be withdrawn.

Based on the above, it is submitted that the application is in condition for allowance and notice of such, with allowed claims 1 and 3-20, is earnestly solicited.

Should the Examiner believe that a conference would help to expedite the prosecution of this application, the Examiner is encouraged to contact the undersigned counsel to arrange for such an interview.

Respectfully submitted,

September 21, 2004
Date

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